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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,719	03/11/2004	Christian Herzum	1890-0066	5006

7590 05/19/2005

Maginot, Moore & Beck
Suite 3000
111 Monument Circle
Indianapolis, IN 46204

EXAMINER	
PERALTA, GINETTE	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,719	HERZUM ET AL.	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Ozaki et al. (U. S. Pat. 5,094,965).

Regarding claim 1, Ozaki et al. teaches in Fig. 2L a semiconductor device that comprises a substrate 1; an active area *(8a, 8b)* formed within the substrate 1; a first non-planar metallization level *(9, 19b)* which is formed on the substrate and is in contact with the active area; and a second planar metallization level *50* arranged spaced apart from the first metallization level via a through connection *14b*.

Regarding claim 2, Ozaki et al. discloses in Fig. 2L that the semiconductor device further comprises a field effect transistor having a gate 4, a source area 8*a*, and a drain area 8*b*, wherein the first non-planar metallization level includes a first portion *9* connected to the source area *6a*, a second portion *19b* connected to the drain area *8b* and a third portion *9* at least partially covering the gate, and wherein the second planar metallization level includes at least one portion connected to the second portion *19b* of the first non-planar metallization level.

Regarding claim 3, Ozaki et al. discloses in Fig. 2L that the first portion *9* and the third portion *9* of the first non-planar metallization level are connected.

Regarding claim 4, Ozaki et al. discloses in Fig. 2L that between the first non-planar metallization level *(9 and 19b)* and the second planar metallization level *50* an insulating layer *12* is arranged, wherein in the insulating layer *12* at least one through connection *14b* for a connection of the first non-planar metallization level to the second planar metallization level is formed.

Regarding claim 5, the structure of Ozaki et al. including a third portion of a first non-planar metallization level connected to the drain region inherently results in the shielding of the gate against electrostatic or electrodynamic interferences.

Regarding claim 6, Ozaki et al. discloses in Figs. 2L and 3 an amplifier circuit comprising a field effect transistor that comprises a substrate 1; an active area formed within the substrate comprising a gate *4*, a source area *6b*; and a drain area *6a*; a first non-planar metallization level *(9 and 19b)* which is formed on the substrate and is in contact with the active area; and a second planar metallization level *50* arranged spaced apart from the first metallization level above the substrate and connected to the first metallization level *(9 and 19b)* via a through connection *14b*; and wherein the first non-planar metallization level *(9 and 19b)* includes a first portion *9* connected to the source area *6a*, a second portion *19b* connected to the drain area *6b*; and a third portion *9* at least partially covering the gate, and wherein the second planar metallization level *50*

includes at least one portion connected to the second portion *19b* of the first non-planar metallization level.

Regarding claim 7, Ozaki et al. discloses in Fig. 2L that the first portion *9* and the third portion *9* of the first non-planar metallization level are connected.

Regarding claim 8, Ozaki et al. discloses in Fig. 2L that between the first non-planar metallization level *(9 and 19b)* and the second planar metallization level *50* an insulating layer *12* is arranged, wherein in the insulating layer *12* at least one through connection *14b* for a connection of the first non-planar metallization level to the second planar metallization level is formed.

Regarding claim 9, the structure of Ozaki et al. including a third portion of a first non-planar metallization level connected to the drain region inherently results in the shielding of the gate against electrostatic or electrodynamic interferences.

Regarding claim 10, Ozaki et al. discloses in Fig. 2L that the semiconductor device further comprises a field effect transistor having a gate *4*, a source area *8a*, and a drain area *8b*, wherein the first non-planar metallization level includes a first portion *19b* connected to the source area *8b*, a second portion *9* connected to the drain area *8a*, and a third portion *9* at least partially covering the gate, and wherein the second planar metallization level *50* includes at least one portion connected to the first portion *19b* of the first non-planar metallization level.

Regarding claim 11, Ozaki et al. discloses in Fig. 2L that the first portion *9* and the third portion *9* of the first non-planar metallization level are connected.

Regarding claim 12, Ozaki et al. discloses in Fig. 2L that between the first non-planar metallization level *(9 and 19b)* and the second planar metallization level *50* an insulating layer *12* is arranged, wherein in the insulating layer *12* at least one through connection *14b* for a connection of the first non-planar metallization level to the second planar metallization level is formed.

Regarding claim 13, the structure of Ozaki et al. including a third portion of a first non-planar metallization level connected to the drain region inherently results in the shielding of the gate against electrostatic or electrodynamic interferences.

Regarding claim 14, Ozaki et al. discloses in Fig. 2L, a semiconductor device comprising a substrate *1;* active areas formed within the substrate *1* comprising a source area and a drain area *(8a and 8b);* a gate *4* disposed between the source area and the drain area and insulated from the substrate by an oxide layer *3;* a first non-planar metallization level *(9 and 19b)* formed on the substrate in contact with the active areas, including a first portion connected to the source area, a second portion connected to the drain area, and a third portion at least partially covering the gate, the third portion including a portion extending downwardly between the gate and the second portion and terminating at an end displaced from the substrate by a displacement *18;* and a second planar metallization level *50* arranged spaced apart from the first metallization level above the substrate and connected to the second portion of the first metallization level *19b* via a through connection *14b.*

Regarding claim 11, Ozaki et àl. discloses in Fig. 2L that the first portion *9* and the third portion *9* of the first non-planar metallization level are connected.

Regarding claim 16, Ozaki et al. discloses in Fig. 2L that between the first non-planar metallization level *(9 and 19b)* and the second planar metallization level *50* an insulating layer *12* is arranged, wherein in the insulating layer *12* at least one through connection *14b* for a connection of the first non-planar metallization level to the second planar metallization level is formed.

Regarding claim 17, the structure of Ozaki et al. including a third portion of a first non-planar metallization level connected to the drain region inherently results in the shielding of the gate against electrostatic or electrodynamic interferences.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki et al..

Regarding claim 18, Ozaki et al. discloses the claimed invention with the exception disclosing the distance between the third portion and the second portion and

the displacement, but it discloses that the second portion is in relative close distance to the third portion.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the distance between the third and second portions of the metallization level as there is no statement denoting the criticality of the distance between the third and second portions, and as long that the two portions do not coincide therefore affecting the operation of the device.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Regarding claim 19, Ozaki et al. discloses in Fig. 2L that the device further comprises an oxide layer *5*.

Regarding claim 20, Ozaki et al. discloses in Fig. 2L that the structure further comprises a reduced surface field area *6b* formed in the substrate and disposed between the gate *4* and the drain area *8b*.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571) 272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP

Wael Fahmy
SPE 2814